Complete circuit

The complete circuit diagram of the stereo decoder is shown in figure 4. The MPX stereo signal is first amplified by T1, and fed via capacitor C3 to the input of the IC (pin 1). The free-running frequency of the VCO is determined by R5, R6, P2 and C10. The 228 kHz VCO signal is available externally (at pin 15) for test and alignment purposes. The manual mono/stereo switch is connected to pin 9 of the IC, and the stereo indicator LED is connected via R8 to pin 7. When the decoder is switched to mono operation, the oscillator is disabled. This eliminates the possibility of interference due to the oscillator signal if the decoder is used in a combined AM/FM receiver. The channel separation of the decoder is determined by the potential at pin 11 (point B). The relationship between channel separation and the voltage at this point is illustrated in figure 5. The voltage can be varied over a range between approximately 0.5 and 2 V by potentiometer P4. The advantage of continuously variable channel separation is that it then becomes possible to reach a compromise between channel separation and signal-to-noise ratio of the audio signal. In the case of a weak transmitter and a noisy stereo signal one can reduce the channel separation to the point where one obtains relatively noise-free reception.

The components for the lowpass filter which provides the DC control voltage for the VCO are connected between pins 13 and 14. The lowpass filter for the second detector is somewhat simpler and requires only a single external component, C6. The de-emphasis networks for the left and right channel signals are formed by C8/R12 and C9/R11 respectively.

T2 and T3 are buffer amplifiers which provide approximately 6 dB of gain. The pilot tone filter, Toko type BLR 3107N, contains two identical but separate LC networks for the rejection of the 19 kHz pilot tone frequency and the 38 kHz subcarrier. The response of the filter is shown in figure 6. This filter is pre-tuned at the factory and requires no further adjustment.

Finally, each channel is provided with an output buffer in the form of a JFET op-amp (IC2 and IC3).

Printed circuit board

The component overlay and track pattern of the printed circuit board for the decoder circuit are shown in figure 7. Construction should not present any particular problems, the only point to watch being the length of the wiring to the mono/stereo switch. Since the capacitance between pin 9 of the IC and earth must not exceed 100 pF, the wiring should be kept as short as possible. Of course, S1 can also be omitted, if so desired, although particulary in fringe reception areas it is often useful to be able to switch to mono in order to obtain less noisy reception.

It is also possible to omit P4, in which case the channel separation will be permanently at maximum.

Alignment

1. First of all the gain of T1 is increased to maximum by setting P1 for zero resistance.
2. Assuming that the IF stage of the tuner has already been aligned, tune to stereo transmission and adjust P2 until the stereo indicator lamp (D1) lights up. Generally speaking, the lamp should remain lit over a fairly wide range of setting for P2. With P2 set to the middle of this range, reduce the gain of T1 by increasing the resistance of P1 slightly, and

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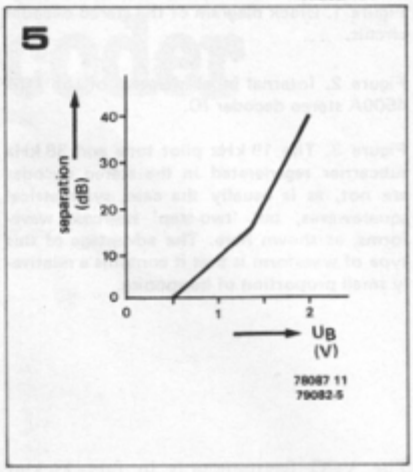

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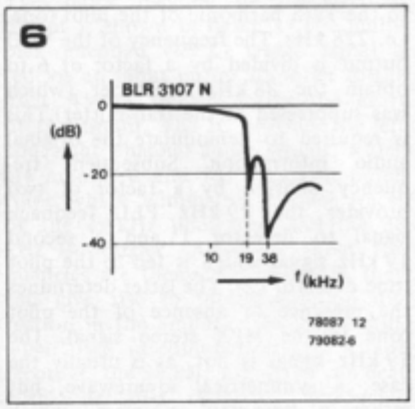

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